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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,752	02/11/2004	Christopher D.W. Jones	JONES 4-22-67	3615

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EXAMINER	
PHAM, HOAI V	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 08/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,752	JONES ET AL.	
	Examiner	Art Unit	
	Hoai v Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11 February 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 8-9, and 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Quek et al. [U.S. Pat. 5,744,853].

With respect to claim 1, Quek et al. (figs. 2b, 3b, 4b, 5b and cols. 4-9) discloses a method of forming a semiconductor device, comprising:

simultaneously forming first electrodes (40a) adjacent each other on a substrate (30) (see fig. 3b);

forming a dielectric layer (42b) between the first electrodes (40a) (see fig. 4b); and

creating a second electrode (46b") between the first electrodes (40a), the second electrode (46b") contacting the dielectric layer (42b) between the first electrodes to thereby form adjacent interdigitated electrodes (see fig. 5b).

With respect to claim 2, Quek et al. discloses producing a first conductive layer (38) over the substrate (30) prior to simultaneously forming and wherein simultaneously forming includes simultaneously forming the first electrodes (40a) on the first conductive

layer (38), the conductive layer interconnecting the first electrodes (see fig. 3b, col. 6, lines 20-65).

With respect to claim 3, Quek et al. discloses that forming a dielectric layer (42b) includes forming the dielectric layer (42b) over and between the first electrodes (40a) and creating a second electrode (46b") includes creating an electrode layer over and between the first electrodes to form interconnected second electrodes over and between the first electrodes (see fig. 5b, col. 7, lines 52-59 and col. 8, lines 56-67).

With respect to claims 4 and 9, Quek et al. discloses that simultaneously forming includes patterning a sacrificial layer on the substrate, forming the first electrodes (40a) adjacent each other within the patterned sacrificial layer and on the substrate, and removing the sacrificial layer (see fig. 3b and col. 7, lines 14-36).

With respect to claim 5, Quek et al. discloses that producing a first conductive layer (38) over the substrate prior to simultaneously forming and wherein simultaneously forming includes patterning a sacrificial layer on the substrate (30), forming the first electrodes adjacent each other within the patterned sacrificial layer and on the substrate, and removing the sacrificial layer (see figs. 2b, 3b; col. 6, lines 20-67 and col. 7, lines 14-36).

With respect to claim 8, Quek et al. (figs. 2b, 3b, 4b, 5b, 7 and cols. 4-9) discloses a method of manufacturing an integrated circuit, comprising:

forming active or passive devices over a substrate (30);

creating an interdigitated capacitor over the substrate, including:

placing a first conductive layer (36) over the substrate (30) (see fig. 2b),

simultaneously forming first electrodes (40a) adjacent each other on the first conductive layer (36), the first conductive layer (36) interconnecting the first electrodes (40a) (see fig. 3b),

forming a dielectric layer (42b) over and between the first electrodes (40a) and on the first conductive layer (36) (see fig. 4b), and

depositing an electrode layer (46b") over and between the first electrodes (40a), the second electrode (46b") to form interconnected second electrode (46b") over and between the first electrodes (see fig. 5b); and

interconnecting the active or passive devices and the interdigitated capacitor by a contact stud (56) to form an operative integrated circuit (see fig. 7).

With respect to claim 12, Quek et al. discloses that forming a dielectric layer (42b) includes forming a dielectric layer (silicon nitride) having a high dielectric constant (see col. 8, lines 1-2).

With respect to claims 13-14, Quek et al. discloses the first electrodes (40a), the first conductive layer (36), and the electrode layer (46b") are comprised of substantially the same material (see col. 5, lines 50-53 and col. 8, lines 56-59).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quek et al. [U.S. Pat. 5,744,853] in view of Shih et al. [U.S. Pat. 6,436,787] Applicant IDS.

Quek et al. discloses all the limitation as claimed above except: a first barrier layer located between the first electrodes and the dielectric layer; and a second barrier layer located between the dielectric layer and the second electrodes. However, Shih et al. discloses the first barrier layer (26) located between the first electrodes (24) and the dielectric layer (28), and a second barrier layer (30) located between the dielectric layer and the second electrodes (34) to prevent copper ions from diffusing into the dielectric

layer thereby reducing the leakage current (see fig. 3, col. 3, lines 10-46). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to incorporate the first and second barrier layers as taught by Shih et al. into the device of Gupta et al. in order to reduce the leakage current (see col. 3, lines 10-46).

6. Claims 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quek et al. [U.S. Pat. 5,744,853].

Quek et al. does not teach the exact an aspect ratio range of their first electrode, as claimed by Applicant. However, the aspect ratio range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoai Pham
Patent Examiner